Remarks/Arguments

Applicants thank the Examiner for a thorough and timely examination and for considering the references submitted in the Information Disclosure Statement on November 12, 2008.

I. Status of Claims

Claims 1-16 and 33-34 are currently pending in the application. This amendment amends claim 1, and addresses each point of objection and rejection raised by the Examiner.

The amended claim language finds support in the specification as originally filed. No new matter has been added. Favorable reconsideration is respectfully requested.

II. Rejections of the Claims under 35 U.S.C. §112, 1st Paragraph

Claims 1-16, 33 and 34 are rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. Specifically, the Examiner states that "nowhere does the specification teach wherein the symbol codes are written in the format of a $2^m * J$ matrix." The Examiner's rejection is unclear, as line 12 on page 10 – line 5 of page 14 of the present specification clearly discloses this feature. Applicants assume the Examiner may be rejecting the language of "symbol codes", which appears to be a typographical error. Accordingly, Applicants amend claim 1 to recite "code symbols" instead of "symbol codes." The term "code symbols" is consistent with the claims and specification. Applicants respectfully

request the Examiner to reconsider and withdraw the rejections of claims 1-16 and 33-34 under 35 U.S.C. 112, first paragraph.

III. Rejections of the Claims under 35 U.S.C. §112, 2nd Paragraph

Claims 1-16, 33 and 34 are rejected under 35 U.S.C. 112, second paragraph as allegedly failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Claims 1-16, 33 and 34 are additionally rejected under 35 U.S.C. 112, second paragraph as allegedly being incomplete for omitting essential elements, such omission amounting to a gap between the elements.

First, the Examiner states that "it is not clear how 'assuming that the value of the remainder R is 0' results in a distinguishing step from simply 'generating an interim address by bit reversal order (BRO) operation on an index of a code symbol.'" Applicants respectfully disagree. Nevertheless, claim 1 is newly amended to recite: "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol as if the code symbols constitute a perfect $2^m * J$ matrix." The newly amended feature of claim 1 further distinguishes the step to comply with the requirements of 35 U.S.C. 112, second paragraph. One of ordinary skill in the art would be able to discern the affect of the newly amended assumption on a BRO operation, thus the amendment clearly defines the step of generating an interim address.

Secondly, the Examiner asserts that the term "in accordance with" in claim 1 is a relative term which allegedly renders the claim indefinite. Applicants respectfully disagree. Nevertheless, Applicants amend claim 1 to recite: "calculating an address compensation factor for compensating the interim address based on the number of the

R code symbols written in the last column J." The newly amended claim 1 clearly defines the step of compensating an address compensation factor, such that there is no indefiniteness in the scope of the claimed feature.

Additionally, the Examiner asserts that the language "the real value of the remainder R" lacks sufficient antecedent basis. As provided above in newly amended claim 1, the rejected language has been removed. Therefore, this rejection is moot in view of the newly amended claim.

Finally, the Examiner rejects claims 1-16, 33 and 34 under 35 U.S.C. 112, second paragraph, as allegedly being incomplete for omitting essential steps. Specifically, the Examiner states that "nowhere does claim 1 recite the connection between 'reading the code symbol written in the generated read address' and decoding 'encoder packet in a receiver for a mobile communication system supporting interleaving.'" Accordingly, Applicants amend claim 1 to further recite the step of "decoding the code symbol read from the generated read address." The newly amended step clearly bridges the alleged gap between the steps.

Applicants submit that the amendments to claim 1 and the arguments and clarification provided above necessarily render claims 1-16 and 33-34 specific and definite under 35 U.S.C. 112, second paragraph. Accordingly, Applicants respectfully request withdrawal of the rejections to claims 1-16 and 33-34 under 35 U.S.C. §112 second paragraph.

IV. Rejections of the Claims under 35 U.S.C. §101

Claims 1-16, 33 and 34 are rejected under 35 U.S.C. 101 as allegedly being directed to non-statutory subject matter, specifically as being directed to an abstract mathematical algorithm.

Despite the detailed arguments presented in the response filed December 12, 2008, the Examiner maintains that claim 1 is non-statutory for allegedly being "directed to an abstract mathematical algorithm of generating an abstract binary address number value intended for use in a (sic) abstract method for reading data intended for use in implementing an abstract algorithm for rearranging data." Applicants respectfully disagree. Nevertheless, in order to advance prosecution of the present application, Applicants amend claim 1 as discussed above to recite the step of decoding the code symbol read from the generated read address. The Examiner repeatedly argues that calculating an address to read abstract data out of a matrix array does not provide any utility. Newly amended claim 1 necessarily provides utility of the method in a real world application of decoding an encoder packet in a receiver. As such, newly amended claim 1 is necessarily directed to statutory subject matter in compliance with 35 U.S.C. 101 and does not attempt to gain a patent on every "substantial practical application" of an abstract mathematical algorithm, as alleged by the Examiner. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejections of claims 1-16, 33 and 34 under 35 U.S.C. 101.

V. Rejections of the Claims under 35 U.S.C. §102(b)

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as allegedly being anticipated by TIA/EIA/IS-2000.2-A-1. Applicants respectfully request reconsideration and withdrawal of these rejections.

Applicants respectfully disagree with the Examiner's interpretation of the applied reference. The Examiner cites footnote 12 on page 2-111 of TIA/EIA/IS-2000.2-A-1 for allegedly teaching a sequence of length N_{turbo} being mapped to 2^{n+4} + R positions in a 2^5 x 2^n array where R is the number of remainder bits exceeding the first 2^{n-1} columns and partially filling the remaining array. Even if the Examiner's interpretation is correct, in no way does such a disclosure teach any feature in as complete detail as claimed in claim 1. Specifically, the alleged code symbols in TIA/EIA/IS-2000.2-A-1 are not written in a 2^m * J matrix where R is the number of remaining bits in the last column J. As stated by the Examiner, R in TIA/EIA/IS-2000.2-A-1 is the number of bits exceeding the first 2^{n-1} columns. Therefore, in an array of 2^n columns, R must partially fill 2^{n-1} columns. Clearly, this teaching cannot be equated with the claimed feature discussed above.

The Examiner also states that TIA/EIA/IS-2000.2-A-1 allegedly teaches the step of generating an interim address by bit reversal order (BRO) operation on an index of a code symbol assuming the value of the remainder R is 0, as shown in Fig 2.1.3.1.4.2.3-1 and step 6 on page 2-111. Applicants respectfully disagree. The method of TIA/EIA/IS-2000.2-A-1 performs bit reversal on the 5 least significant bits of a counter value, which necessarily cannot be considered the same as the claimed index of a code symbol. Further, the Examiner cites step 5 on page 2-111 of

TIA/EIA/IS-2000.2-A-1 as teaching a step of calculating an address compensation factor for compensating the interim address in accordance with a column formed with the real value of the remainder R, however, as discussed above, TIA/EIA/IS-2000.2-A-1 fails to teach at least the same remainder as claimed. Therefore, TIA/EIA/IS-2000.2-A-1 cannot teach at least the calculation of an address compensation factor for accounting for the R code symbols written in the last column J. Additionally, TIA/EIA/IS-2000.2-A-1 generates an output address by appending (as least significant bits) the alleged n address compensation bits to the 5 least significant bits of a counter value that were bit reversed, resulting in an output address of 5 + n bits. Clearly, this step cannot be considered the same as adding an interim address and an address compensation factor as recited in claim 1.

In view of the above arguments, TIA/EIA/IS-2000.2-A-1 clearly fails to teach each feature of at least claim 1 in as complete detail as claimed. Accordingly, Applicants request the Examiner to reconsider and withdraw the rejections of claims 1 and 2 under 35 U.S.C. 102(b).

VI. Double Patenting Rejection

Claim 1 is rejected on the ground of nonstatutory double patenting over claim 5 of U.S. Patent No. 6,668,350. Applicants respectfully disagree with the Examiner's interpretation of Kim and the claim language and further maintain the arguments presented in previously filed responses.

Specifically, Applicants believe that the Examiner clearly does not fully comprehend the scope of the present application and its relation to the cited art. Kim clearly does not disclose or suggest at least the step of calculating an address

compensation factor for compensating the interim address to account for the R code symbols written in the last column J. The Examiner states that Kim discloses the generating the read address by adding to the interim address (BRO(K/J)) the address compensation factor (2^m(K mod J)). Newly amended claim 1 clearly recites a step of calculating an address compensation factor based on the number of the R code symbols written in the last column J. Kim, however, is directed to an interleaving method in which there are no remaining R bits. Thus, any interleaving in Kim is performed with a complete uniform matrix. Since there are no remaining R bits in a last column, Kim cannot disclose a compensation factor based on the remaining R bits. The Examiner states that Kim explicitly recites "calculating a third variable r corresponding to a remainder obtained by dividing a reading sequence K by the second variable J." Such disclosure merely defines the modulo operation which results in the remainder of division of one number by another. The variable 'r' which is the result of (K mod J) cited in Kim is not related in any way to the remainder R as defined in the preamble of claim 1. In systems where the number of bit symbols do not enable a uniform matrix in interleaving, it is necessary to compensate for the remaining bits. The present application recites a method of compensating for these remaining bits, thus resulting in the step of address compensation that is neither apparent nor obvious in view of Kim.

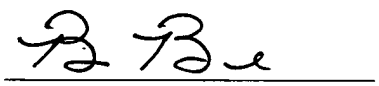
Applicants respectfully believe the Examiner misunderstands both the present application and the cited reference of Kim. Kim is directed to a method for reading code symbols. The read address cited by Kim for reading code symbols, however, does not include any compensation for a remaining number of bits R formed

in the last column that does not complete the last column. Kim fails to disclose generating any read address in situations wherein the number of code symbols is as described in the preamble of claim 1. Thus, at the least, Kim fails to discuss calculating an address compensation factor for compensating the interim address based on the number of the R code symbols written in the last column J, and generating a read address by adding the interim address and the address compensation factor. Since Kim fails to describe or suggest at least these recited features, there is no basis for a double patenting rejection. Applicants respectfully request the Examiner to withdraw the nonstatutory double patenting rejection of claim 1 in view of Kim.

CONCLUSION

In view of the above, it is believed that the above-identified application is in condition for allowance, and notice to that effect is respectfully requested. Should the Examiner have any questions, the Examiner is encouraged to contact the undersigned at the telephone number indicated below. Additionally, Applicants request a one month extension of time under 37 CFR 1.136(a), and submit herewith the applicable fees under 37 C.F.R. §1.17.

Respectfully submitted,



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